8.5 – 10 GHz 10 Watt Power Amplifier

Features

- Frequency Range : 8.5 – 10GHz
- 40 dBm Psat
- 13 dB Power gain
- 25% PAE
- High IP3
- Input Return Loss > 10 dB
- Output Return Loss > 9 dB
- Dual bias operation
- DC decoupled input and output
- 0.5 µm InGaAs pHEMT Technology
- Chip dimension: 5.2 x 5.0 x 0.1 mm

Typical Applications

- RADAR
- Military & space
- LMDS, VSAT

Description

The AMT2144111 is a X-band Power amplifier with 40dBm power output. The PA uses 2 stages of amplification and operates in 8.5 – 10 GHz frequency range. The PA features 13 dB of gain with input and output return losses of 10 dB and 9 dB respectively. The PA has a high IP3 of 47dBm and 25% PAE. This feature enables it to be used in the applications requiring efficiency along with linearity. The chip operates with dual bias supply voltage. The die is fabricated using a reliable 0.5µm InGaAs pHEMT technology. The Circuit grounds are provided through vias to the backside metallization.

Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Absolute Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain bias voltage (Vd)</td>
<td>+10</td>
<td>volts</td>
</tr>
<tr>
<td>Drain current (Id)</td>
<td>4</td>
<td>A</td>
</tr>
<tr>
<td>RF input power (RFin at Vd=9V)</td>
<td>33</td>
<td>dBm</td>
</tr>
<tr>
<td>Operating temperature</td>
<td>-50 to +85</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

1. Operation beyond these limits may cause permanent damage to the component
Electrical Specifications \(^{(1)}\) @ \(T_A = 25\ ^\circ\text{C}\), \(V_{d_1} = V_{d_2} = 8\text{V}\), \(V_{g_1} = V_{g_2} = -1.1\text{V}\) 
\(Z_o = 50\ \Omega\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Typ.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency Range</td>
<td>8.5 – 10 GHz</td>
<td></td>
</tr>
<tr>
<td>Gain</td>
<td>13 dB</td>
<td></td>
</tr>
<tr>
<td>Gain Flatness</td>
<td>+/-0.5 dB</td>
<td></td>
</tr>
<tr>
<td>Output Power (P1 dB)</td>
<td>38.4 dBm</td>
<td></td>
</tr>
<tr>
<td>Input Return Loss</td>
<td>10 dB</td>
<td></td>
</tr>
<tr>
<td>Output Return Loss</td>
<td>9 dB</td>
<td></td>
</tr>
<tr>
<td>Saturated output power (Psat)</td>
<td>40 dBm</td>
<td></td>
</tr>
<tr>
<td>Output Third Order Intercept (IP3)</td>
<td>47 dBm</td>
<td></td>
</tr>
<tr>
<td>Power Added Efficiency (PAE)</td>
<td>25% --</td>
<td></td>
</tr>
<tr>
<td>Supply Current((I_{dsq}))</td>
<td>2.9 A</td>
<td></td>
</tr>
<tr>
<td>Supply Current((I_{dsat})^2)</td>
<td>4.3 A</td>
<td></td>
</tr>
</tbody>
</table>

Note:

1. Electrical specifications as measured in test fixture.
2. \(I_{dsat}\) is the drain current corresponding to saturated output power.
Test fixture data

\[ V_{d1} = V_{d2} = V_d, \quad V_{g1} = V_{g2} = -1.1V, \quad \text{Total Current (Idq)} = 2.9A, \quad T_A = 25^\circ C \]

Output power plotted at \( V_d = 8V \)

![Gain Graph](image)

![Output Power Graph](image)
Test fixture data

\[ V_{d1} = V_{d2} = V_d, \quad V_{g1} = V_{g2} = -1.1V, \quad \text{Total Current (Idq)} = 2.9A, \quad T_A = 25^\circ C \]

Output power plotted at \( V_d = 9V \)
Test fixture data

\( V_{d1} = V_{d2} = 8V, \ V_{g1} = V_{g2} = -1.1V, \ Total \ Current \ (Idq) = 2.9A, \ T_A = 25^\circ C \)
Output Power Plots:

\[ V_{d1} = V_{d2} = 8V, \quad V_{g1} = V_{g2} = -1.1V, \quad \text{Total Current (I_{dsat})} = 4A, \quad \text{Freq} = 9.5GHz, \quad T_A = 25^\circ C \]

\[ V_{d1} = V_{d2} = 9V, \quad V_{g1} = V_{g2} = -1.1V, \quad \text{Total Current (I_{dsat})} = 4A, \quad \text{Freq} = 9.5GHz, \quad T_A = 25^\circ C \]
Temperature data

\[ V_{d1} = V_{d2} = 8V, \quad V_{g1} = V_{g2} = -1.1V, \quad \text{Total Current (Idq)} = 2.9A, \quad T_A = 25^\circ C \]
Temperature data

\[ V_{d1} = V_{d2} = 8V, \quad V_{g1} = V_{g2} = -1.1V, \quad \text{Total Current (Idq) = 2.9A, } T_A = 25^\circ C \]
Bond Pad Locations

Units: millimeters (inches)

Note:
1. All RF and DC bond pads are 100µm x 100µm
2. Pad no. 1 : RF IN
3. Pad no. 3,11 : 1st stage gate voltage (V_{g1})
4. Pad no. 7 : RF Output
5. Pad no. 4,10 : 1st stage drain voltage (V_{d1})
6. Pad no. 5,9 : 2nd stage gate voltage (V_{g2})
7. Pad no. 6,8 : 2nd stage drain voltage (V_{d2})
8. All the dimensions shown above are measured taking bottom left corner as reference.
Recommended Assembly Diagram

**Note:**

1. Open stub of 4mm length, 1mm width and 0.1mm thickness to be placed at output immediate to the chip as shown above for proper matching.
2. Two 1 mil (0.0254mm) bond wires of minimum length should be used for RF input and output.
3. Two 1 mil (0.0254mm) bond wires of minimum length should be used from chip bond pad to 100pF capacitor.
4. Input and output 50 ohm lines are on 5 mil RT Duroid substrate.
5. 100pF,0.1uF and 1uF bypass capacitors are used as shown above.
6. The RF input & output ports are DC decoupled on-chip.
7. Proper heat sink like Copper tungsten or copper molybdenum to be used for better reliability of chip.

**Die attach:** For Epoxy attachment, use of a two-component conductive epoxy is recommended. An epoxy fillet should be visible around the total die periphery. If Eutectic attachment is preferred, use of fluxless AuSn (80/20) 1-2 mil thick preform solder is recommended. Use of AuGe preform should be strictly avoided.

**Wire bonding:** For DC pad connections use either ball or wedge bonds. For best RF performance, use of 150 - 200µm length of wedge bonds is advised. Single Ball bonds of 250-300µm though acceptable, may cause a deviation in RF performance.

**GaAs MMIC devices are susceptible to Electrostatic discharge. Proper precautions should be observed during handling, assembly & testing**

All information and Specifications are subject to change without prior notice.