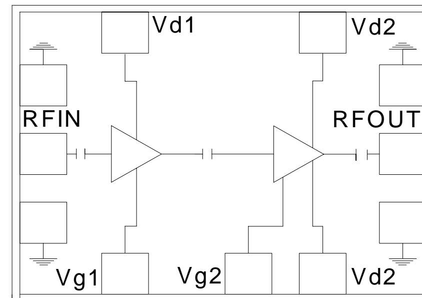
29 - 31 GHz Power Amplifier

Features

- Frequency Range : 29 - 31GHz
- 27 dBm output P1dB
- 11 dB Power gain
- 30% PAE
- High IP3
- Input Return Loss > 7 dB
- Output Return Loss > 10 dB
- Dual bias operation
- No external matching required
- DC decoupled input and output
- 0.15 µm InGaAs pHEMT Technology
- Chip dimension: 2.6 x 1.5 x 0.1 mm

Functional Diagram



Typical Applications

- RADAR
- Military & space
- LMDS, VSAT

Description

The AMT2173021 is a Ka-band Power amplifier with 27dBm power output. The PA uses 2 stages of amplification and operates in 29 - 31 GHz frequency range. The PA features 11 dB of gain with input and output return losses of 7 dB and 10 dB respectively. The PA has a high IP3 of 37dBm and greater than 30% PAE. This feature enables it to be used in the applications requiring efficiency along with linearity. The chip operates with dual bias supply voltage.The die is fabricated using a reliable 0.15µm InGaAs pHEMT technology. The Circuit grounds are provided through vias to the backside metallization.

Absolute Maximum Ratings (1)

Parameter	Absolute Maximum	Units
Drain bias voltage (Vd)	+7	volts
Drain current (Id)	420	mA
RF input power (RFin at Vd=5V)	25	dBm
Operating temperature	-50 to +85	^{o}C
Storage Temperature	-65 to +150	^{o}C

1. Operation beyond these limits may cause permanent damage to the component

Electrical Specifications [1] @ T_A = 25 °C, $V_{d1} = V_{d2}$ = 5V, $V_{g1} = V_{g2}$ = -0.75V Z_o =50 Ω

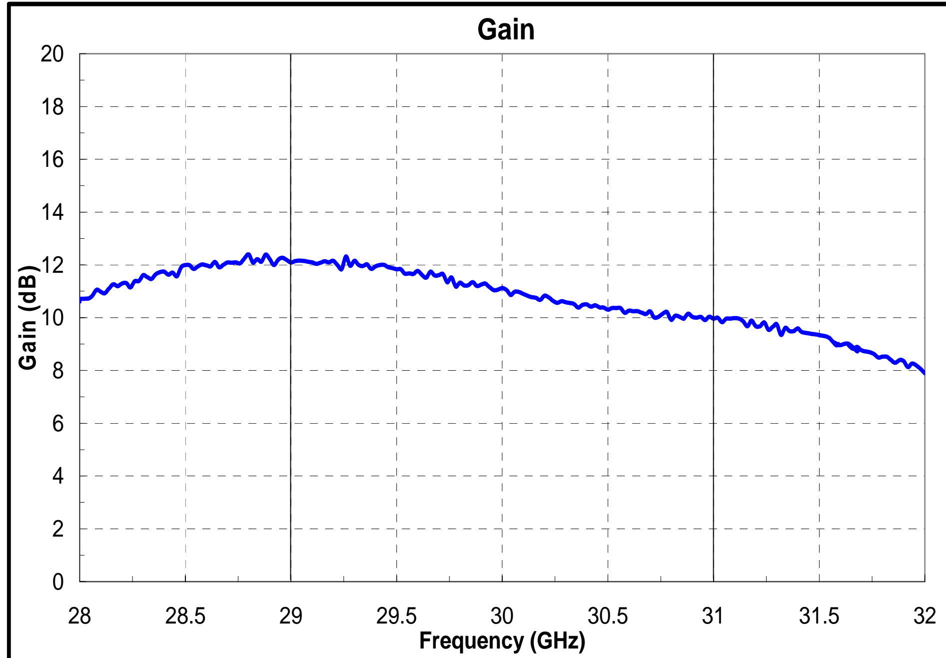
Parameter	Typ.	Units
Frequency Range	29 - 31	GHz
Gain	11	dB
Gain Flatness	+/-1	dB
Output Power (P1 dB)	27	dBm
Input Return Loss	7	dB
Output Return Loss	10	dB
Saturated output power (Psat)	29	dBm
Output Third Order Intercept (IP3)	37	dBm
Power Added Efficiency (PAE)	30%	--
Supply Current	330	mA

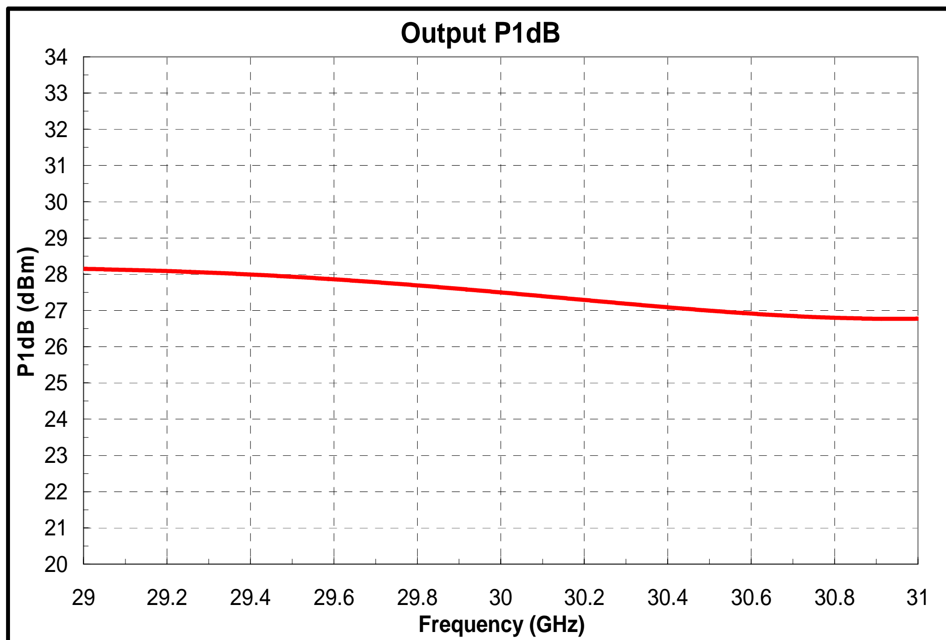
Note:

1. Electrical specifications as measured in test fixture.

Test fixture data

$V_{d1} = V_{d2} = 5V$, $V_{g1} = V_{g2} = -0.75V$, Total Current =330ma, $T_A = 25\,^{o}C$





Test fixture data

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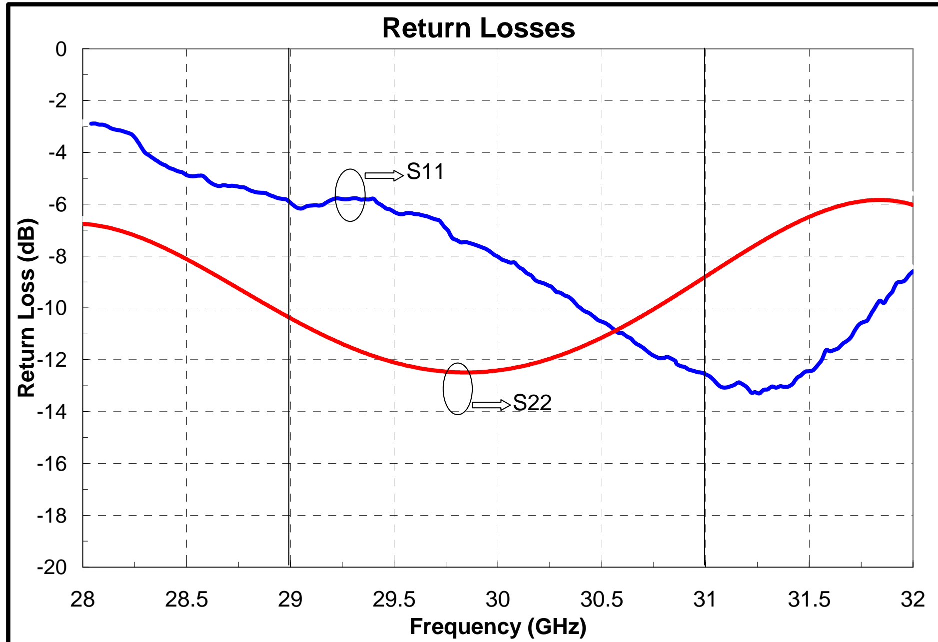

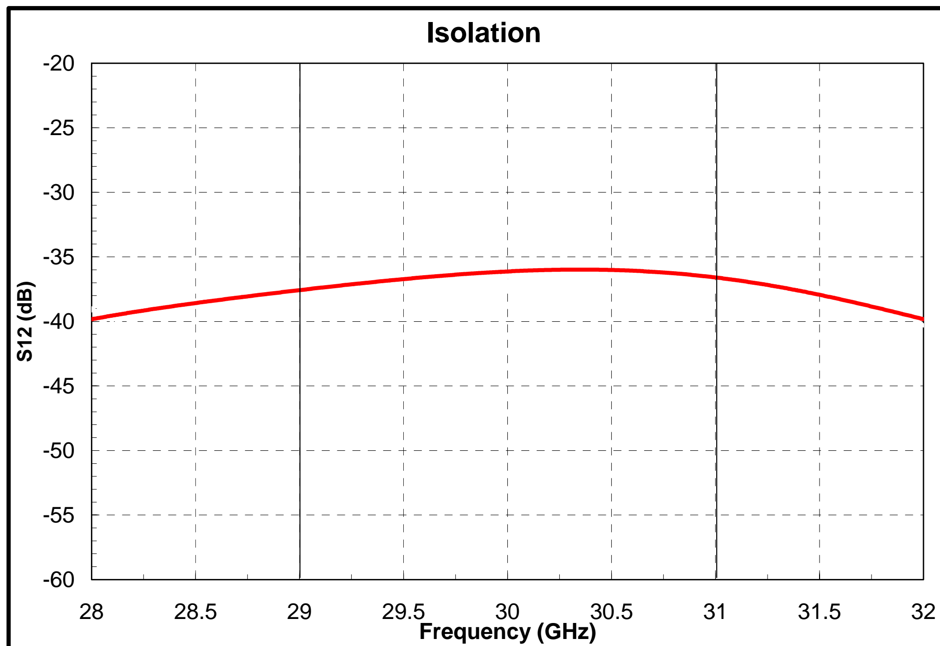

Test fixture data

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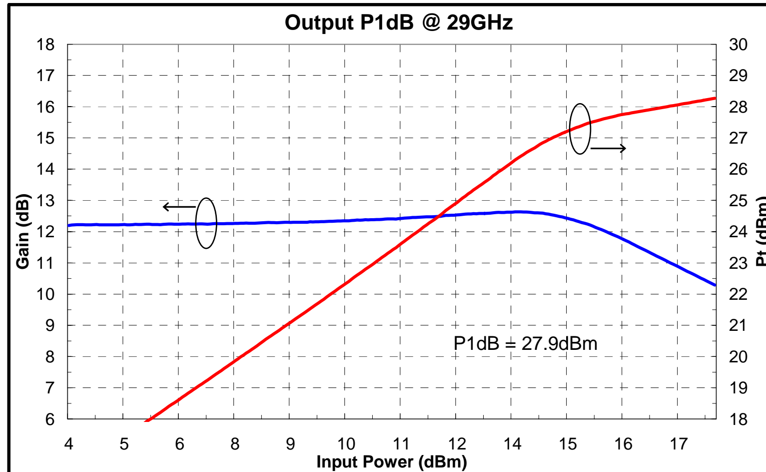
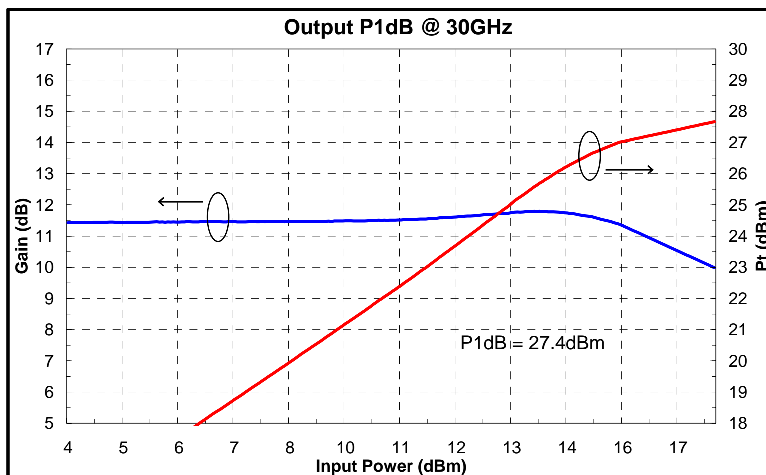
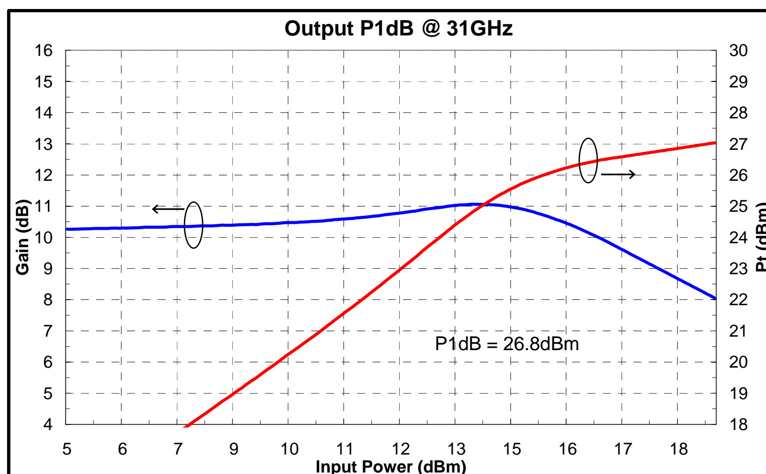
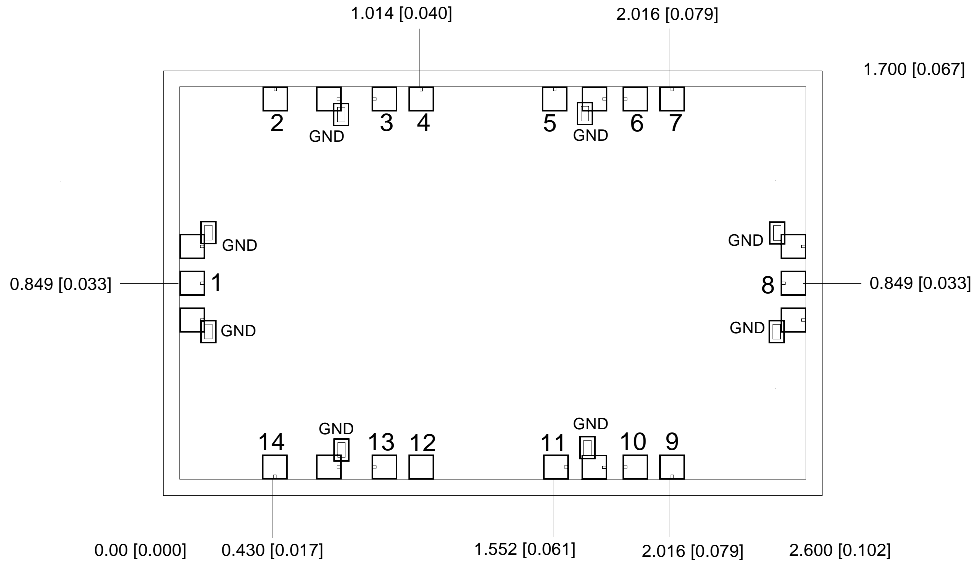






Mechanical Characteristics

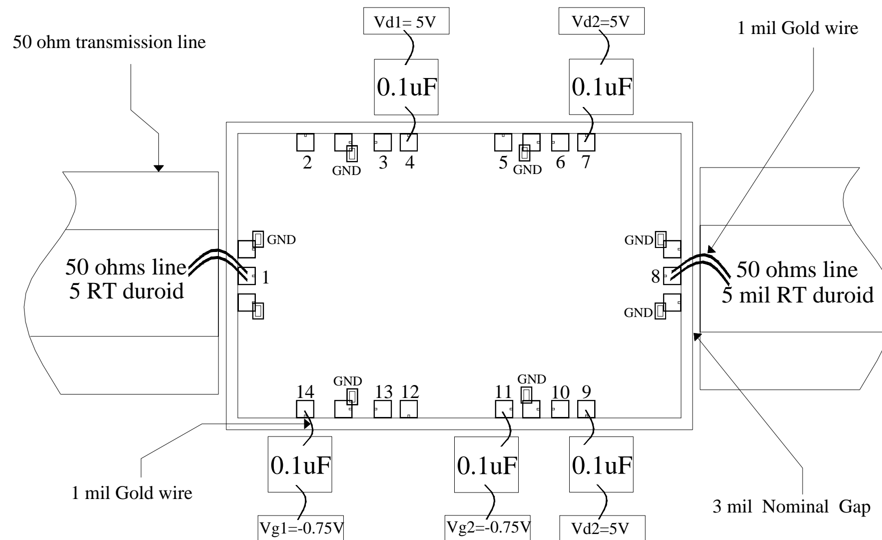


Units: millimeters (inches)

Note:

1. All RF and DC bond pads are 100µm x 100µm
2. Pad no. 1 : RF IN
3. Pad no. 4 : 1st stage drain voltage(V_{d1})
4. Pad no. 8 : RF Output
5. Pad no. 7,9 : 2nd stage drain voltage(V_{d2})
6. Pad no. 11 : 2nd stage gate voltage(V_{g2})
7. Pad no. 14 : 1st stage gate voltage (V_{g1})
8. Pad nos. 2,3,5,6,10,12,13 : NC

Recommended Assembly Diagram



Note :

1. Two 1 mil (0.0254mm) bond wires of minimum length should be used for RF input and output.
2. Two 1 mil (0.0254mm) bond wires of minimum length should be used from chip bond pad to 100pF capacitor.
3. Input and output 50 ohm lines are on 5 mil RT Duroid substrate
4. 0.1 μF capacitors may be additionally used as a second level of bypass for reliable operation
5. The RF input & output ports are DC decoupled on-chip.

Die attach: For Epoxy attachment, use of a two-component conductive epoxy is recommended. An epoxy fillet should be visible around the total die periphery. If Eutectic attachment is preferred, use of fluxless AuSn (80/20) 1-2 mil thick preform solder is recommended. Use of AuGe preform should be strictly avoided.

Wire bonding: For DC pad connections use either ball or wedge bonds. For best RF performance, use of 150 - 200μm length of wedge bonds is advised. Single Ball bonds of 250-300μm though acceptable, may cause a deviation in RF performance.

GaAs MMIC devices are susceptible to Electrostatic discharge. Proper precautions should be observed during handling, assembly & testing

All information and Specifications are subject to change without prior notice

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